* A screenshot of a computer

  Description automatically generatedRCLK Goes High after Data TX with “EUSART\_is\_tx\_done()” as shown below.

Figure 1: RCLK is Early. Should Latch at the end of the transmission. Polling “EUSART\_is\_tx\_ready()” in this example. Trying “EUSART\_is\_tx\_done()” next.

A screenshot of a computer

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Figure 2: RCLK Fixed. QA remains low, however. QH Has strange behavior. Is my USART data flipped around?

A screenshot of a computer

Description automatically generated

Figure 3: QH was only floating, so strange behavior was due to that. Even when flipping the data, QA remains low, so that was not the cause for QA being low after OE goes low.

* For USART, DATA and CLK Rising Edge are in line. Could this be causing the issue? Need to consult Common Line IC Data Sheet.
  + Maybe not since in logic analyzer above, CLK Goes high when SER has been high and QH is zero at the output.
* Appears that the last bit of USART Tx is ignored by the Common Line Register. Need to investigate why.
* Note: Sending 0xFF on TX results in all 9 LEDs Turning on. Logic Analyzer:

A screen shot of a computer

Description automatically generated

Figure 4: Sending All Ones on TX.

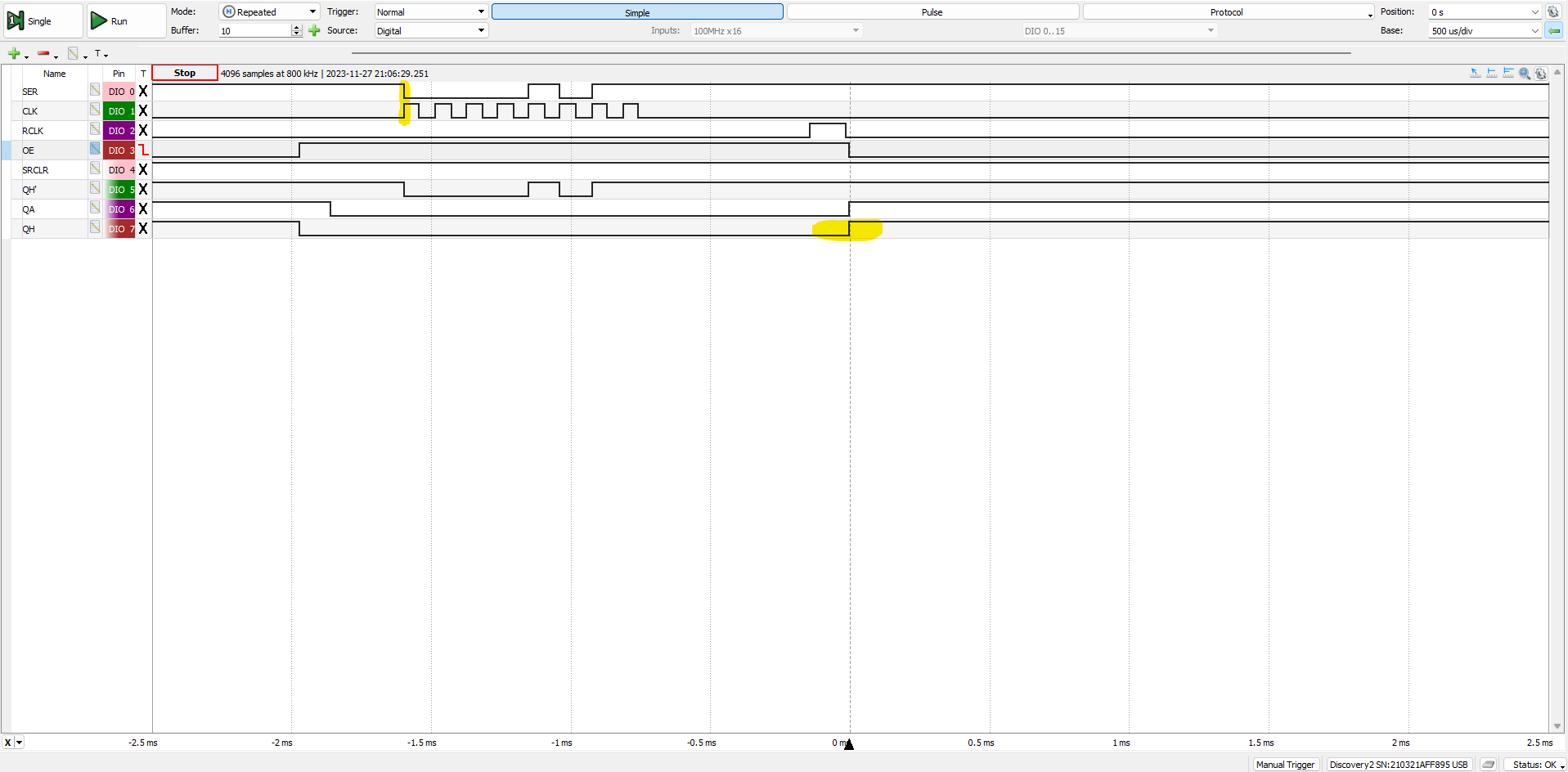


Figure 5: Appears that the offset I am noticing in the output of the shift registers is due to a timing incompatibility between USART and the Common Line Driver Register. 1st Rising Edge of SRCLK erroneously clocks SER in the high state before USART TX begins.

* Changing the clock to negative polarity seems to have fixed this issue. This is necessary because serial data is designed to change on the leading edge of the clock to maximize the time CLK is high during that bit for USART Tx’s. Inverting the clock signal positions CLK rising edge right in the middle of the data which is exactly what is needed. (Figure 6)

A screenshot of a computer

Description automatically generated

Figure : RCLK goes high 283.8 us after USART TX completion in this transmission.

A screenshot of a computer

Description automatically generated

Figure : RCLK goes high 796.3 us after USART TX Completion. That is a difference of 512.5 us (~0.5 ms). There are several different times that RCLK will go high between these two extremes on each cycle of the transmission.

* There are several different times that RCLK will go high between these two extremes on each cycle of the transmission. I think the cause is the code “while(!EUSART\_is\_tx\_done());”. There must be a number of factors that determine how long until the transmission is considered done. Also, this could be an issue caused by the translation between C and ASM. Would interrupts reduce this variation? Does this even matter in the grand scheme of this clock project?
  + Don’t think this issue should matter. Worst case, Access line receive data 0.5 ms later and it takes that much longer for the frame to update.